CLAIMS

1. A method of establishing a time interval in terms of a time taken for a capacitor to charge from a reference voltage level to a detection voltage level, comprising:

supplying at the start of the interval a capacitor charging current, using a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage; and

identifying the detection voltage level to signal the end of the time interval, using a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of variations of the first power supply voltage.

2. The method according to claim 1, wherein the predetermined dependency is a function of the difference between: i) a voltage supplied, from the first power supply voltage, to the first and second semiconductor devices, and ii) a threshold voltage of the first and second semiconductor devices.

3. The method according to claim 1, wherein the first and second semiconductor devices are matched transistors.

4. The method according to claim 1, wherein the first semiconductor device is a transistor having a control input biased by a biasing signal to deliver a constant current.

5. The method according to claim 1, wherein the second semiconductor device comprises a transistor placed in a current flow path passing a current substantially equal to the charging current while the capacitor is being charged.

6. The method according to claim 1, wherein the first and second semiconductor devices are placed in first and second current flow paths controlled to pass substantially the same current during the time interval.

7. The method according to claim 6, wherein the current flow in the first and second current flow paths is controlled by a control signal obtained from respective branches of a current mirror circuit.

8. The method according to claim 6, wherein the first and second current flow paths are controlled by a current mirror circuit formed by two current mirror transistors in respective current branches and connected as back-to-

back transistors, a first current mirror transistor being connected in series with a resistive device to establish a reference current, and a second current mirror transistor being connected in series with a diode connected transistor, and wherein the first semiconductor device is a transistor biased by a signal taken from the common node of the back-to-back transistors and the current passing through the second semiconductor device is controlled by a transistor biased by the common node of the second current mirror transistor and the diode connected transistor.

9. The method according to claim 6, wherein the transistors of the current mirror circuit are MOS transistors.

10. The method according to claim 1, wherein the first and second semiconductor devices are MOS transistors, both MOS transistors having substantially equal threshold voltages and connected to a same power supply voltage.

11. The method according to claim 1, wherein the first and second semiconductor devices are PMOS transistors, both PMOS transistors having substantially equal threshold voltages and connected to a same positive power supply voltage.

12. The method according to claim 1, wherein the reference voltage is at ground potential and the detection voltage corresponds to the first power supply voltage, minus the threshold voltage of the first semiconductor device when in the conducting state.

13. The method according to claim 1, further comprising supplying a detection signal from the second semiconductor device, indicative of the detection of the detection voltage, to a Schmitt trigger set to deliver predetermined logic voltages as a function of the voltage value of the detection signal.

14. The method according to claim 1, wherein:

the first semiconductor device is a first PMOS transistor having a source connected to the first power supply voltage, and a drain connected to a first terminal of the capacitor, the capacitor having a second terminal connected to the reference voltage;

the second semiconductor device is a second PMOS transistor having a source connected to the first power supply voltage, and a drain connected to a drain of a first NMOS transistor, whose source connected to the reference voltage;

the first PMOS transistor and the first NMOS transistor are biased at their gates by respective first and second voltage signals obtained from a current mirror circuit composed of two PMOS current mirror transistors in

respective current branches and connected back-to-back by their gates, a first current mirror transistor being connected in series with a resistive device to establish a reference current, and a second current mirror transistor connected in series with a second NMOS transistor having its drain connected to its gate, the gate of the first PMOS transistor being biased by a signal taken from the common node of the back-to-back transistors, and the gate of the first NMOS transistor being biased by the common node of the second current mirror transistor and the drain of the second NMOS transistor.

15. A method of generating an oscillating signal having a periodicity established by establishing a time interval in terms of a time taken for a capacitor to charge from a reference voltage level to a detection voltage level, the method comprising:

supplying at the start of the interval a capacitor charging current, using a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage;

identifying the detection voltage level to signal the end of the time interval, using a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of the first power supply voltage;

discharging the capacitor to the reference voltage after the second semiconductor device identifies the detection voltage level; and

repeating the supplying, identifying and discharging steps cyclically, and producing the oscillating signal on the basis of the corresponding cyclical detection of the detection voltage level.

16. The method according to claim 15, further comprising: extracting a response signal produced by the second semiconductor device in response to a detection of the detection voltage level, and using the response signal to establish the periodicity of the oscillating signal.

17. The method according to claim 16, further comprising: using the response signal to trigger logic levels changing in correspondence with the periodicity of the response signal, the triggered logic levels forming the oscillator output signal.

18. The method according to claim 15, further comprising: periodically blocking a supply of current to the capacitor by using a switching means in the current supply path at a given point between the first terminal of the capacitor and the first power supply voltage, the switching means being responsive to a periodic signal generated from the detection signal.

19. The method according to claim 15, further comprising: periodically discharging the capacitor by using a switchable capacitor discharging means that selectively connects the first terminal of the capacitor to the reference voltage to discharge the capacitor, the switchable capacitor discharging means being responsive to a periodic signal generated from the detection signal.

20. A method of generating an oscillating signal having a periodicity established by a time taken for a capacitor to charge from a reference voltage to a detection voltage level, the method comprising:

providing first and second time bases, each comprising:

means for supplying a capacitor with a charging current, comprising a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage,

means for identifying the detection voltage level to signal the end of the time interval, comprising a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of the first power supply voltage, and

means for discharging the capacitor to the reference voltage after the second semiconductor device identifies the detection voltage level;

causing the first and second time bases to operate in alternation by initially starting the charging of the capacitor of the first time base, and cyclically using the detection of the detection voltage of the first time base to both start the charging of the capacitor of the second time base and to discharge the capacitor of the first time base;

using the detection of the detection voltage of the second time base to both start the charging of the capacitor of the first time base and to discharge the capacitor of the second time base; and

using the resulting cyclic detection of a detection voltage at one or both time bases as a time base to produce the oscillating signal.

21. A method of generating an oscillating signal having a periodicity established by a time taken for a capacitor to charge from a reference voltage to a detection voltage level, comprising:

providing first and second time bases, each comprising:

means for supplying a capacitor with a charging current, comprising a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage,

means for identifying the detection voltage level to signal the end of the time interval, comprising a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of the first power supply voltage, and

means for discharging the capacitor to the reference voltage after the second semiconductor device identifies the detection voltage level; and

performing cyclical steps a) to d) below:

a) charging the capacitor of the first time base through the first semiconductor device thereof,

b) in response to the second semiconductor device of the first time base signalling the detection of the detection voltage value,

charging the capacitor of the second time base through the first semiconductor device of the second time base,

c) discharging the capacitor of the first time base to the reference voltage while the capacitor of the second time base is being charged,

d) in response to the second semiconductor device of the second time base signalling the detection of the detection voltage value, returning to cyclical step a) and discharging the capacitor of the second time base prior to cyclical step b),

thereby producing the oscillating signal on the basis of the cyclical alternation of detecting the detection voltage by the first and/or the second time base(s).

22. The method according to claim 21, further comprising the step of providing logic gating circuit means for causing the detection of the detection voltage by the first time base to trigger cyclical steps b) and c), and for causing the detection of the detection voltage by the second time base to trigger cyclical step d) and, after a first cycle, cyclical step a).

23. The method according to claim 21, further comprising the steps of providing switching means at each of the first and second time bases, in the first current path, the switching means of the first time base being responsive

to a detection of the detection voltage by the second time base for preventing a supply of current to the capacitor of the first time base, and

the switching means of the second time base being responsive to a detection of the detection voltage by the first time base for preventing a supply of current to the capacitor of the second time base.

24. The method according to claim 21, further comprising, selectively connecting the first terminal of a respective capacitor to the reference voltage to discharge the capacitor for each of the first and second time bases, by a switchable capacitor discharging means,

the switchable capacitor discharging means of the first time base being responsive to a detection of the detection voltage by the second semiconductor device of the first time base to connect the first terminal of the capacitor of the first time base plate to the reference voltage, and

the switchable capacitor discharging means of the second time base being responsive to a detection of the detection voltage by the second semiconductor device of the second time base to connect the first terminal of the capacitor of the second time base plate to the reference voltage.

25. A device for establishing a time interval in terms of a time taken for a capacitor to charge from a reference voltage level to a detection voltage level, comprising:

means for supplying at the start of the interval a capacitor charging current, comprising a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage; and

means for identifying the detection voltage level to signal the end of the time interval, comprising a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of variations of the first power supply voltage.

26. The device according to claim 25, wherein the predetermined dependency is a function of the difference between: i) a voltage supplied, from the first power supply voltage, to the first and second semiconductor devices, and ii) a threshold voltage of the first and second semiconductor devices.

27. The device according to claim 25, wherein the first and second semiconductor devices are matched transistors.

28. The device according to claim 25, wherein the first semiconductor device is a transistor having a control input biased by a biasing signal to deliver a constant current.

29. The device according to claim 25, wherein the second semiconductor device comprises a transistor placed in a current flow path controllable to pass a current substantially equal to the charging current while the capacitor is being charged.

30. The device according to claim 25, wherein the first and second semiconductor devices are placed in first and second current flow paths controllable to pass substantially the same current during the time interval.

31. The device according to claim 30, wherein the current flow in the first and second current flow paths is controllable by a control signal obtained from respective branches of a current mirror circuit.

32. The device according to claim 30, wherein the first and second current flow paths are controllable by a current mirror circuit formed by two current mirror transistors in respective current branches and connected as back-to-back transistors, a first current mirror transistor being connected in series with a resistive device to establish a reference current, and a second current mirror transistor being connected in series with a diode connected transistor, and

wherein the first semiconductor device is a transistor biased by a signal taken from the common node of the back-to-back transistors and the current passing through the second semiconductor device is controlled by a transistor biased by the common node of the second current mirror transistor and the diode connected transistor.

33. The device according to claim 32, wherein the transistors of the current mirror circuit are MOS transistors.

34. The device according to claim 25, wherein the first and second semiconductor devices are MOS transistors, both MOS transistors having substantially equal threshold voltages and connected to a same power supply voltage.

35. The device according to claim 25, wherein the first and second semiconductor devices are PMOS transistors, both PMOS transistors having substantially equal threshold voltages and connected to a same positive power supply voltage.

36. The device according to claim 25, wherein the reference voltage is at ground potential and the detection voltage corresponds to the first power supply voltage, minus the threshold voltage of the first semiconductor device when in a conducting state.

37. The device according to claim 25, further comprising means for supplying a detection signal from the second semiconductor device, indicative of the detection of the detection voltage, to a Schmitt trigger set to deliver predetermined logic voltages as a function of the voltage value of the detection signal.

38. The device according to claim 25, wherein:

the first semiconductor device is a first PMOS transistor having a source connected to the first power supply voltage, and a drain connected to a first terminal of the capacitor, the capacitor having a second terminal connected to the reference voltage;

the second semiconductor device is a second PMOS transistor having a source connected to the first power supply voltage, and a drain connected to a drain of a first NMOS transistor, whose source connected to the reference voltage;

the first PMOS transistor and the first NMOS transistor are biased at their gates by respective first and second voltage signals obtained from a current mirror circuit composed of two PMOS current mirror transistors in respective current branches and connected back-to-back by their gates, a first current mirror transistor being connected in series with a resistive device to establish a reference current, and a second current mirror transistor connected in series with a second NMOS transistor having its drain connected to its gate, the gate of the first PMOS transistor being biased by a signal taken

from the common node of the back-to-back transistors, and the gate of the first NMOS transistor being biased by the common node of the second current mirror transistor and the drain of the second NMOS transistor.

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39. A device for generating an oscillating signal having a periodicity established by establishing a time interval in terms of a time taken for a capacitor to charge from a reference voltage level to a detection voltage level, comprising:

means for supplying at the start of the interval a capacitor charging current, using a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage;

means for identifying the detection voltage level to signal the end of the time interval, using a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of the first power supply voltage;

means for discharging the capacitor to reference voltage after the second semiconductor device identifies the detection voltage level; and

means for cyclically operating the means for supplying, means for identifying, and means for discharging, to produce the oscillating signal on the basis of the corresponding cyclical detection of the detection voltage level.

40. The device according to claim 39, further comprising means for extracting a response signal produced by the second semiconductor device in

response to a detection of the detection voltage level, and means for using the response signal to establish the periodicity of the oscillator output signal.

41. The device according to claim 39, further comprising means for using the response signal to trigger logic levels changing in correspondence with the periodicity of the response signal, the triggered logic levels forming a clock signal.

42. The device according to claim 39, further comprising switching means in the current supply path at a given point between the first terminal of the capacitor and the first power supply voltage, the switching means being responsive to a periodic signal generated from the detection signal for periodically blocking a supply of current to the capacitor.

43. The device according to claim 39, further comprising switchable capacitor discharging means for selectively connecting the first terminal of the capacitor to the reference voltage to discharge the capacitor, the switchable capacitor discharging means being responsive to a periodic signal generated from the detection signal for periodically discharging the capacitor.

44. A device for generating an oscillating signal having a periodicity established by a time taken for a capacitor to charge from a reference voltage to a detection voltage level, comprising:

first and second time bases, each comprising:

means for supplying a capacitor with a charging current, comprising a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage,

means for identifying the detection voltage level to signal the end of the time interval, comprising a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of the first power supply voltage, and

means for discharging the capacitor to the reference voltage after the second semiconductor device identifies the detection voltage level; and

control means for causing the first and second time bases to operate in alternation by initially starting the charging of the capacitor of the first time base, the control means being operative for cyclically:

using the detection of the detection voltage of the first time base to both start the charging of the capacitor of the second time base and to discharge the capacitor of the first time base, and

using the detection of the detection voltage of the second time base to both start the charging of the capacitor of the first time base and to discharge the capacitor of the second time base; and

means responsive to the resulting cyclic detection of a detection voltage at one or both time bases as a time base to produce the oscillating signal.

45. A device for generating an oscillating signal having a periodicity established by a time taken for a capacitor to charge from a reference voltage to a detection voltage level, comprising:

first and second time bases, each comprising:

means for supplying a capacitor with a charging current, comprising a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage;

means for identifying the detection voltage level to signal the end of the time interval, comprising a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of the first power supply voltage; and

means for discharging the capacitor to the reference voltage after the second semiconductor device identifies the detection voltage level; and

means for performing cyclical steps a) to d) below:

a) charging the capacitor of the first time base through the first semiconductor device thereof;

b) in response to the second semiconductor device of the first time base signalling the detection of the detection voltage value,

charging the capacitor of the second time base through the first semiconductor device of the second time base;

c) discharging the capacitor of the first time base to the reference voltage while the capacitor of the second time base is being charged; and

d) in response to the second semiconductor device of the second time base signalling the detection of the detection voltage value, returning to cyclical step a) and discharging the capacitor of the second time base prior to cyclical step b),

thereby producing the oscillating signal on the basis of the cyclical alternation detecting the detection voltage by the first and/or the second time base(s).

46. The device according to claim 45, further comprising the step of providing logic gating circuit means for causing the detection of the detection voltage by the first time base to trigger cyclical steps b) and c), and for causing the detection of the detection voltage by the second time base to trigger cyclical step d) and, after a first cycle, cyclical step a).

47. The device according to claim 46, further comprising switching means at each of the first and second time bases, in the first current path, the switching means of the first time base being responsive to a detection of the

detection voltage by the second time base for preventing a supply of current to the capacitor of the first time base, and

the switching means of the second time base being responsive to a detection of the detection voltage by the first time base for preventing a supply of current to the capacitor of the second time base.

48. The device according to claim 47, further comprising, for each of the first and second time bases, switchable capacitor discharging means for selectively connecting the first terminal of a respective the capacitor to the reference voltage to discharge the capacitor,

the switchable capacitor discharging means of the first time base being responsive to a detection of the detection voltage by the second semiconductor device of the first time base to connect the first terminal of the capacitor of the first time base plate to the reference voltage, and

the switchable capacitor discharging means of the second time base being responsive to a detection of the detection voltage by the second semiconductor device of the second time base to connect the first terminal of the capacitor of the second time base plate to the reference voltage.

49. An oscillator for generating an oscillating signal waveform substantially immediately after supplying power to the oscillator, comprising:

a time base circuit for establishing a time interval in terms of a time taken for a capacitor to charge from a reference voltage level to a detection voltage level, the time base circuit comprising:

means for supplying at the start of the interval a capacitor charging current, comprising a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage; and

means for identifying the detection voltage level to signal the end of the time interval, comprising a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of variations of the first power supply voltage, and

wherein an initial half wave of a waveform generated by the oscillator starting substantially at a normal point in the phase of the waveform, the initial half wave having a duration substantially equal to a cycle period of the waveform.

50. An oscillator for generating an oscillating signal waveform substantially immediately after supplying power to the oscillator, comprising:

a time base circuit for generating an oscillating signal having a periodicity established by establishing a time interval in terms of a time taken for a capacitor to charge from a reference voltage level to a detection voltage level, the time base circuit comprising:

means for supplying at the start of the interval a capacitor charging current, using a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage;

means for identifying the detection voltage level to signal the end of the time interval, using a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of the first power supply voltage;

means for discharging the capacitor to reference voltage after the second semiconductor device identifies the detection voltage level; and

means for cyclically operating the means for supplying, means for identifying, and means for discharging, to produce the oscillating signal on

the basis of the corresponding cyclical detection of the detection voltage level, and

wherein an initial half wave of a waveform generated by the oscillator starting substantially at a normal point in the phase of the waveform, the initial half wave having a duration substantially equal to a cycle period of the waveform.

51. An oscillator for generating an oscillating signal waveform substantially immediately after supplying power to the oscillator, comprising:

a time base circuit for generating an oscillating signal having a periodicity established by a time taken for a capacitor to charge from a reference voltage to a detection voltage level, the time base circuit comprising:

first and second time bases, each comprising:

means for supplying a capacitor with a charging current, comprising a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage,

means for identifying the detection voltage level to signal the end of the time interval, comprising a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of the first power supply voltage, and

means for discharging the capacitor to the reference voltage after the second semiconductor device identifies the detection voltage level; and

control means for causing the first and second time bases to operate in alternation by initially starting the charging of the capacitor of the first time base, the control means being operative for cyclically:

using the detection of the detection voltage of the first time base to both start the charging of the capacitor of the second time base and to discharge the capacitor of the first time base, and

using the detection of the detection voltage of the second time base to both start the charging of the capacitor of the first time base and to discharge the capacitor of the second time base; and

means responsive to the resulting cyclic detection of a detection voltage at one or both time bases as a time base to produce the oscillating signal, and

wherein an initial half wave of a waveform generated by the oscillator starting substantially at a normal point in the phase of the waveform, the initial half wave having a duration substantially equal to a cycle period of the waveform.

52. An oscillator for generating an oscillating signal waveform substantially immediately after supplying power to the oscillator, comprising:

a time base circuit for generating an oscillating signal having a periodicity established by a time taken for a capacitor to charge from a reference voltage to a detection voltage level, the time base circuit comprising:

first and second time bases, each comprising:

means for supplying a capacitor with a charging current, comprising a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage;

means for identifying the detection voltage level to signal the end of the time interval, comprising a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of the first power supply voltage; and

means for discharging the capacitor to the reference voltage after the second semiconductor device identifies the detection voltage level; and

means for performing cyclical steps a) to d) below:

a) charging the capacitor of the first time base through the first semiconductor device thereof;

b) in response to the second semiconductor device of the first time base signalling the detection of the detection voltage value, charging the capacitor of the second time base through the first semiconductor device of the second time base;

c) discharging the capacitor of the first time base to the reference voltage while the capacitor of the second time base is being charged; and

d) in response to the second semiconductor device of the second time base signalling the detection of the detection voltage value, returning to cyclical step a) and discharging the capacitor of the second time base prior to cyclical step b),

thereby producing the oscillating signal on the basis of the cyclical alternation detecting the detection voltage by the first and/or the second time base(s), and

wherein an initial half wave of a waveform generated by the oscillator starting substantially at a normal point in the phase of the waveform, the initial half wave having a duration substantially equal to a cycle period of the waveform.

53. An apparatus comprising:

an interface that can be coupled with a second apparatus to exchange therewith data at a data rate according to an oscillating frequency of an oscillating signal wavefrom;

an oscillator, coupled with the interface, for generating the oscillating signal waveform substantially immediately after power is supplied to the oscillator; and

a time base circuit, coupled with the oscillator, for establishing a time interval in terms of a time taken for a capacitor to charge from a reference voltage level to a detection voltage level, the time base circuit comprising:

means for supplying at the start of the interval a capacitor charging current, comprising a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage; and

means for identifying the detection voltage level to signal the end of the time interval, comprising a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of variations of the first power supply voltage, and

wherein the apparatus, substantially immediately after being coupled with the second apparatus and receiving power, exchanges with the second apparatus data at a data rate according to the oscillating frequency of the oscillating signal waveform generated from the oscillator.

54. The apparatus of claim 53, wherein the oscillator receives power from the second apparatus via the interface, and wherein the apparatus, substantially immediately upon being coupled to the second apparatus via the interface exchanges with the second apparatus data at a data rate according to the oscillating frequency of the oscillating signal waveform generated from the oscillator.

55. An apparatus comprising:

an interface that can be coupled with a second apparatus to exchange therewith data at a data rate according to an oscillating frequency of an oscillating signal wavefrom;

an oscillator, coupled with the interface, for generating the oscillating signal waveform substantially immediately after power is supplied to the oscillator; and

a time base circuit, coupled with the oscillator, for establishing a time interval in terms of a time taken for a capacitor to charge from a reference voltage level to a detection voltage level, the time base circuit comprising:

means for supplying at the start of the interval a capacitor charging current, using a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage;

means for identifying the detection voltage level to signal the end of the time interval, using a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of the first power supply voltage;

means for discharging the capacitor to reference voltage after the second semiconductor device identifies the detection voltage level; and

means for cyclically operating the means for supplying, means for identifying, and means for discharging, to produce the oscillating signal on the basis of the corresponding cyclical detection of the detection voltage level, and

wherein the apparatus, substantially immediately after being coupled with the second apparatus and receiving power, exchanges with the second apparatus data at a data rate according to the oscillating frequency of the oscillating signal waveform generated from the oscillator.

56. The apparatus of claim 55, wherein the oscillator receives power from the second apparatus via the interface, and wherein the apparatus, substantially immediately upon being coupled to the second apparatus via the interface exchanges with the second apparatus data at a data rate according to the oscillating frequency of the oscillating signal waveform generated from the oscillator.

57. An apparatus comprising:

an interface that can be coupled with a second apparatus to exchange therewith data at a data rate according to an oscillating frequency of an oscillating signal wavefrom;

an oscillator, coupled with the interface, for generating the oscillating signal waveform substantially immediately after power is supplied to the oscillator; and

a time base circuit, coupled with the oscillator, for establishing a time interval in terms of a time taken for a capacitor to charge from a reference voltage level to a detection voltage level, the time base circuit comprising:

first and second time bases, each comprising:

means for supplying a capacitor with a charging current, comprising a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage,

means for identifying the detection voltage level to signal the end of the time interval, comprising a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of the first power supply voltage, and

means for discharging the capacitor to the reference voltage after the second semiconductor device identifies the detection voltage level; and

control means for causing the first and second time bases to operate in alternation by initially starting the charging of the capacitor of the first time base, the control means being operative for cyclically:

using the detection of the detection voltage of the first time base to both start the charging of the capacitor of the second time base and to discharge the capacitor of the first time base, and

using the detection of the detection voltage of the second time base to both start the charging of the capacitor of the first time base and to discharge the capacitor of the second time base; and

means responsive to the resulting cyclic detection of a detection voltage at one or both time bases as a time base to produce the oscillating signal, and

wherein the apparatus, substantially immediately after being coupled with the second apparatus and receiving power, exchanges with the second apparatus data at a data rate according to the oscillating frequency of the oscillating signal waveform generated from the oscillator.

58. The apparatus of claim 57, wherein the oscillator receives power from the second apparatus via the interface, and wherein the apparatus, substantially immediately upon being coupled to the second apparatus via the

interface exchanges with the second apparatus data at a data rate according to the oscillating frequency of the oscillating signal waveform generated from the oscillator.

59. An apparatus comprising:

an interface that can be coupled with a second apparatus to exchange therewith data at a data rate according to an oscillating frequency of an oscillating signal wavefrom;

an oscillator, coupled with the interface, for generating the oscillating signal waveform substantially immediately after power is supplied to the oscillator; and

a time base circuit, coupled with the oscillator, for establishing a time interval in terms of a time taken for a capacitor to charge from a reference voltage level to a detection voltage level, the time base circuit comprising:

first and second time bases, each comprising:

means for supplying a capacitor with a charging current, comprising a first semiconductor device supplied from a first power supply voltage, the device delivering the charging current to the capacitor according to a predetermined dependency on the first power supply voltage;

means for identifying the detection voltage level to signal the end of the time interval, comprising a second semiconductor device supplied from the first power supply voltage, the second semiconductor device identifying the detection voltage level value according to the same predetermined dependency on the first power supply voltage as for the first semiconductor device, whereby the time interval is made substantially independent of the first power supply voltage; and

means for discharging the capacitor to the reference voltage after the second semiconductor device identifies the detection voltage level; and

means for performing cyclical steps a) to d) below:

a) charging the capacitor of the first time base through the first semiconductor device thereof;

b) in response to the second semiconductor device of the first time base signalling the detection of the detection voltage value, charging the capacitor of the second time base through the first semiconductor device of the second time base;

c) discharging the capacitor of the first time base to the reference voltage while the capacitor of the second time base is being charged; and

d) in response to the second semiconductor device of the second time base signalling the detection of the detection voltage value, returning to cyclical step a) and discharging the capacitor of the second time base prior to cyclical step b),

thereby producing the oscillating signal on the basis of the cyclical alternation detecting the detection voltage by the first and/or the second time base(s), and

wherein the apparatus, substantially immediately after being coupled with the second apparatus and receiving power, exchanges with the second apparatus

data at a data rate according to the oscillating frequency of the oscillating signal waveform generated from the oscillator.

60. The apparatus of claim 59, wherein the oscillator receives power from the second apparatus via the interface, and wherein the apparatus, substantially immediately upon being coupled to the second apparatus via the interface exchanges with the second apparatus data at a data rate according to the oscillating frequency of the oscillating signal waveform generated from the oscillator.